INTERNET SWITCHING BY SATELLITE: AN ULTRA FAST PROCESSOR WITH RADIO BURST SWITCHING.

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RESUME : Résumé français.

Cet article présente une nouvelle approche de la commutation de données de type « paquets Internet » à bord de satellites impliqués dans des systèmes maillés. Héritage du monde de l'optique, le concept « Radio Burst Switching » (RBS) combine les caractéristiques transparente mais statique de la commutation circuit avec la flexibilité du multiplexage statistique. Ceci afin de mieux faire face à la demande croissante de ressource des utilisateurs d'Internet et au besoin de connectivité. L'idée fondatrice du RBS est justifiée par le fait qu'une commutation de type « paquet régénératif » n'exploite en fait qu'une petite partie des données traitées : l'entête de paquet ; tandis que le contenu utile des paquets (charge principale) n'est pas lu. Ainsi, le concept RBS se propose t'il de séparer les informations dites du plan de contrôle (e.g : en-têtes) du reste des donnée utiles (plan de données). Chacun de ces plans transitant sur des chemins séparés, mais reliés. Des gains attendus sur la masse et la consommation électrique sont ainsi attendus grâce à un dimensionnement optimisé de la partie traitement au trafic de contrôle, tandis que les données utiles sont simplement aiguillées avec peu ou pas de traitement.

C'est pourquoi, le concept RBS peut être une solution aux exigences des scénarios « nouvelle génération » de systèmes satellites maillés large bande (centaines de faisceaux, + de 20GHz de bande à commuter). L'intégration du concept dans un environnement DVB-RCS serait possible grâce à une organisation judicieuse des canaux de contrôle et de données et à un traitement embarqué sélectif de la signalisation. De nombreux défis devront être relevés pour l'implémentation du processeur , les principaux portant sur le besoin d'interconnections haut débit ainsi que le recours intensif aux traitements à base de mémoire. Basée sur l'utilisation de transceivers (Multigigabit MGT) et sur une architecture de commutation multi étages, on peut affirmer que la faisabilité d'un commutateur de paquets ultra rapide sera faisable à l'aide des technologies de 2010, tandis que 5 ans auparavant cela ne l'était pas.

Ce papier est issus des travaux préliminaires du projet ULISS. L'objectif du projet est de développer et démontrer la faisabilité à la fois du concept RBS mais aussi d'un processeur de commutation de paquets ultra rapide.

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ABSTRACT : *English abstract*

This article introduces a new switching approach for satellite involved in routing statistical traffic such as IP data. Inherited from the optical domain, Radio Burst Switching (RBS) can combine a coarse switching granularity (such as circuit switching) with a statistical multiplexing (such as packet switching) to cope better with the increasing bandwidth demands of Internet traffic and need for high connectivity. The basic idea of RBS is justified by the fact that for achieving a packet switching mission, the processing is operating on the only small sized header, while the main burden of data does not require processing. Then, in RBS, it is proposed to split the header-like information (control plane) from the useful data (data plane), each one travelling on separated but linked paths. Savings on embedded mass and power can be achieved because the processing stage is sized to the only header traffic, while the data is simply switched without or few processing.

That is the reason why RBS could be a solution for the next generation of broadband satellite system requirements (hundred beams, more than 20GHz of switched bands). Thanks to relevant data and control channels organisation and selective on board regeneration of signalling, it could be possible to integrate RBS into a DVB-RCS environment. Under this scenario, processor implementation is considered as very challenging, mainly due to the interconnect power cost and memory intensive processings. Based on integrated multi gigabit transceivers (MGT) and multi stage switch architecture, it could be confirmed than an ultra fast packet switch will feasible using year 2010 technologies, while it was not 5 years ago.

This paper presents ULISS project upstream activities. Main ULISS goal is to develop and demonstrate the feasibility both of the RBS concept and of an ultra fast packet switch processor.

1 - INTRODUCTION

One of the major challenges of future telecommunication satellites is to efficiently provide wideband connectivity between a high number of user beams (~100 spotbeams, > 20GHz of switched bands). Until now, flexible and dynamic switching systems such as regenerative packet switches have been band-limited, due to the constraints of embedded technology in charge of processing the whole data packet flow. Switching wider bands by satellite has meant reducing flexibility for the benefit of wideband transparent circuit switches - with a resulting reduction in reactivity and connectivity.

This paper presents and develops a new concept called the Radio Burst Switching (RBS), where the processing power is devoted to the only demodulation and decoding of header part of the packet. Then, the system capacity is increased because the main burden of data flow is not processed (demodulation + decoding) but simply switched.

This principle will be first exposed and justified. Integration into a satellite system with wideband beams is developed, addressing DVB-RCS synchronisation and terminal issues. A corresponding ultra fast packet switch processor is presented with associated enabling

technologies, mainly based on integrated multi gigabit transceivers (MGT) and multi stage switch architecture. Thanks to mass and power evaluations, feasibility evolution with time is drawn up, proving that RBS could be an viable solution to future Multimedia missions in Ka Band.

2 - THE RADIO BURST SWITCHING PRINCIPLE AND JUSTIFICATION.

Existing technique providing large band transparent connectivity (generally known as "SS-TDMA" circuit switching) offers quasi-static connectivity for a limited number of beams, under a "user-to-network control centre" connected scheme. In this case, it is easy to understand that this solution is poorly adapted to an increasing number of IP users that generate unpredictable traffic profile. This problem has been solved by the introduction of the packet switching, where the packets are statistically switched on board once the destination header is retrieved. The counter part is the need for embedded processing capability that seriously reduces the bandwidth, in order to achieve the whole packet demodulation and decoding.

Radio Burst Switching by satellite, presented and patented by Alcatel Space [1], has been inspired by the recent Optical Burst Switching (OBS) terrestrial solutions [2], [3]. Optical Burst Switching is seen as a viable switching technology to Terabit backbone networks; it allows the data packets to be switched entirely in the optical domain (e.g λ-switching) without opto-electro-optic conversion, while the header (e.g: destination address) is processed in the electronic domain to determine optimal resource allocation.

Some analogies can be drawn between the OBS and RBS domains, taking advantage of the separation of forwarding (data) and regenerative (header) paths. This separation for satellite switching is justified for transmissions as well as mass & power reasons. First, the data path is waveform-independent, future enhancements to transport formats (modulation schemes, coding, etc.) could be easily upgraded. Secondly, RBS intrinsically minimizes the costly "regenerative" section because only headers are subject to DDD[1] processing, while the bulk of data flows travel on-board transparently with few processing (demultiplexing only).

In the RBS domain, it is proposed to manage variable length and bandwidth data bursts, segmented into fixed slotted packets called burst segments (or packets). Fixed-length burst segments are needed to allow end-to-end system synchronization between the ingress earth stations, the satellite core switch, and the egress earth stations. These burst segments are emitted to fit in specific time periods separated by a guard time (see Figure 1). During the guard time, the satellite-switching plan is updated for the next slotted time period.

[1] demultiplexing/demodulation/Decoding +reverse operations

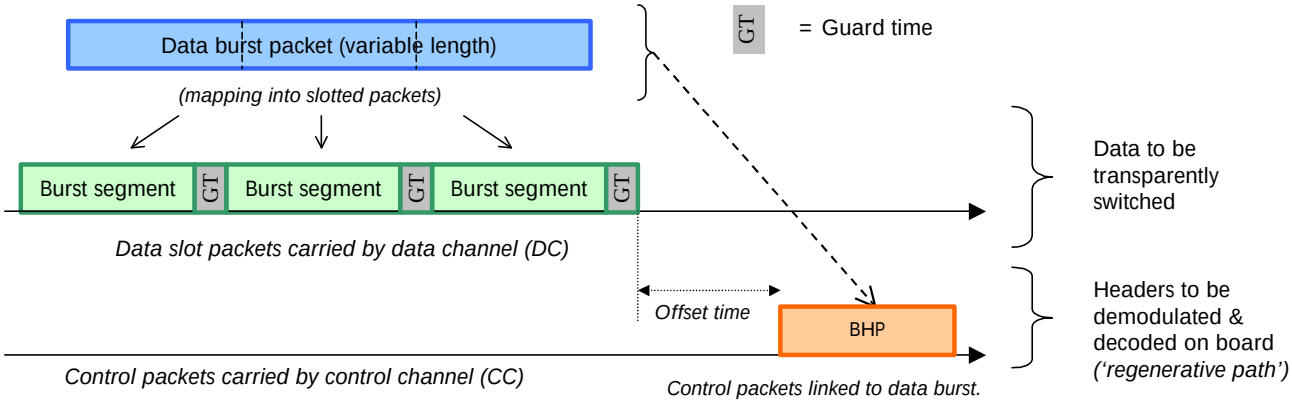

Figure 1: Burst segmentation and its associated BHP

The role of the BHPs (burst header packet) is to inform the satellite switch controller in advance as to when, from where, and to where a data burst will arrive on board. Therefore BHPs are first demodulated and decoded to retrieve error-free information. The embedded controller (see Figure 11) handles the whole flow of BHP requests in real time, scheduling each down-link time slot allocation according to the destination address by using priority and QoS rules carried in the BHP.

3 - TYPICAL SYSTEM SCENARIO.

The scenario proposed is derived from ESA's vision on the next generation of broadband satellite systems ([4], [5]) and is based on a broadband mesh network satellite system providing point-to-point and point-to-multipoint communications. The aim is to provide to system users the means to establish direct (single hop) mesh connection between each other through a bi-directional telecommunication links.

Considering these future generations of systems where hundred of Gbps of throughput are expected to be switched, RBS is quite justified in minimizing the amount of processed bandwidth and then to save mass and power on board.

3.1 - GENERAL SATELLITE SYSTEM DESCRIPTION:

It is proposed to integrate the envisaged satellite system into mechanisms, protocols, messages and information formats based on the Digital Video Broadcasting Return Channel Satellite (DVB-RCS) standard.

Nevertheless, some modifications of this standard should be taken into account due to the specificities of the processor with radio burst switching, enabling the data transmission from one satellite terminal to another within only a single satellite hop. The described satellite system supports 96 beams, with a frequency reuse factor of 4 in the up and down-link, 250 MHz of bandwidth being associated with each beam. Figure 2 displays the proposed beam organization over Europe and Figure 3 displays the power radiated in the down-link by an antenna as presented in [6] towards each point of the coverage area.

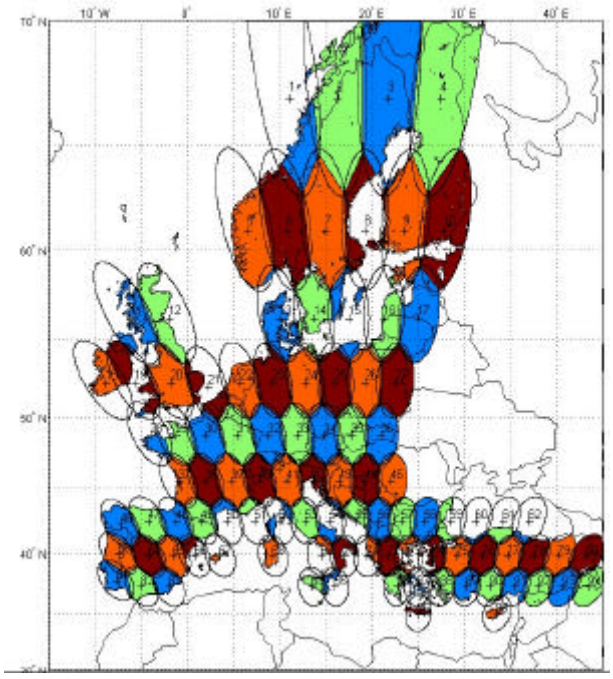

Figure 2 : Proposed coverage area and beam organization with a frequency reuse factor of 4**.**

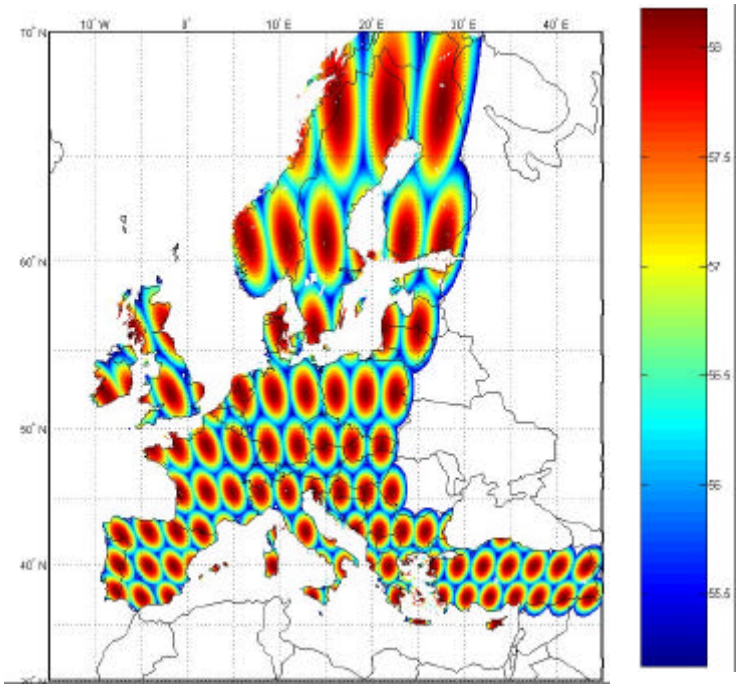

Figure 3: Power radiated by the antenna towards each point of the coverage area in DBi.

In each up-link beam, the 250 MHz available bandwidth is split into 2 sub-bands, due to the terminals limitations to only receive and transmit in a 125 MHz band (see 3.6 -). 88 channels are managed in each up-link sub-band considering carriers with a useful symbol rate of 800ksps. Among these channels 4 are reserved to transmit forward link signalling as defined in DVB-RCS and 6 to carry the specific on-board processing signalling, as explained in section 3.3 -. Therefore, 78 channels are available in each up-link sub-band for data transmission. In down-link, similar computation have lead to take into account 92 channels among which 85 are dedicated to data transmission.

3.2 - COMPARISON WITH CLASSICAL SATELLITE SYSTEMS.

The comparison deals with bent-pipe satellite. It is schematically represented in Figure 4. Classical satellite systems compliant with DVB-RCS provide return link capacities to terminals and a connection to a centralised gateway. The bandwidth resource is partitioned among the overall set of terminals. The Digital Video Broadcasting Satellite (DVB-S) compliant forward link is used to forward information flows (both signalling and data) to the whole community of terminals. In such systems, Satellite Terminal to Satellite Terminal connections can be supported by means of a double satellite hop data transmission.

In the satellite system with radio burst switching, all terminals should access the up-link resources as described in DVB-RCS (Multiple Frequency, Time Division Multiple Access, MF-TDMA). Because the satellite is transparent, the format of all the data bursts and most of the signalling bursts should be the same in the down-link as in the up-link. The concept of forward and return link is not relevant in this case for data transmission. At control plane, the classical DVB-RCS return and forward link signalling should nevertheless be supported for logon, synchronization and up-link resource management purposes. Then, channels will be organised is order to propose a selective processing of signalling on board.

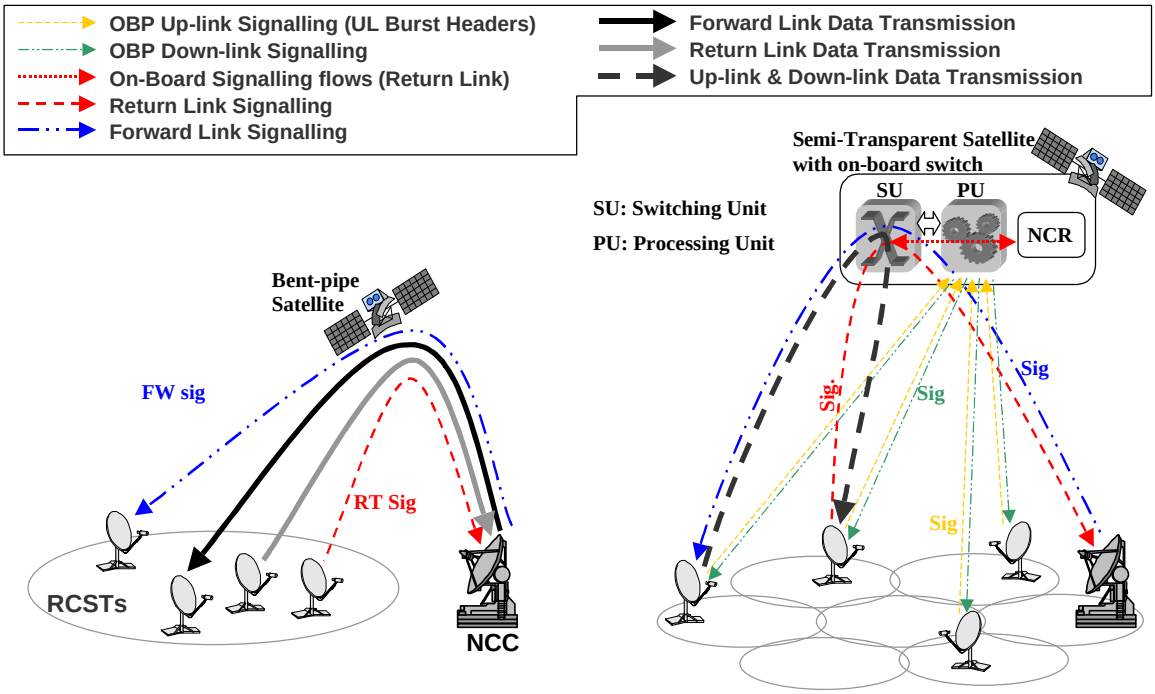

Figure 4: Information flows comparison between a classical DVB-RCS/DVB-S compliant satellite system with bent pipe satellite and the considered satellite system with radio burst switching.

3.3 - ORGANISATION OF THE UP-LINK AND DOWN-LINK RESOURCES

The on-board processor should be transparent at data layer, meaning that bursts of data are neither demodulated nor decoded on-board. Nevertheless, because this data should be switched on-board, information about these data bursts (Quality of Service, destination) are transmitted to the processor over dedicated control channels (CC). These channels are demodulated, decoded and processed on-board. This information is used by the switch controller to attribute down-link resources. One control channel is associated with a given group of data channels (DCG). Over the control channel, during each time slot, all the BHP should be transmitted together with other signalling addressed to controller (eg. required for logon or synchronisation procedures). The BHP should be sent a bit ahead of the associated traffic data bursts. This time offset is required to let enough time to the on-board controller to process the received bursts headers BHP.

A burst header transmission technique is also applied in the down-link to advertise terminals about the location in the down-link Time Division Multiplex (TDM) of the bursts destined to them.

3.4 - ON-BOARD SWITCHING PRINCIPLE.

In the considered satellite system, up and downlink beams are composed of several frequency channels (MF-TDM). Each beam is split into sub bands. A terminal can solely access to one sub-band.

Contenting access to a given terminal destination can be solved by the channel multiplexing technique. In this case, the contending channels are sent at the same time to the terminal and there is no need to buffer on board the data bursts. Of course, it is assumed that the terminal could receive simultaneously several channels. The interest of this technique is to save complexity on board, because the need of buffering is reduced. But some limitations on terminals exist and will be developed in 3.6 -.

The proposed on-board switch relies upon this channel multiplexing technique. At higher layer, its behaviour can be modelled thanks to a channel multiplexing switch. Each input and output of the switch corresponds to one up-link or down-link sub-band respectively. Channel multiplexing switches are basically circuit switches enabling the connection between any up-link carrier and any down-link carrier. The concept of channel multiplexing switching is schematically illustrated in Figure 5.

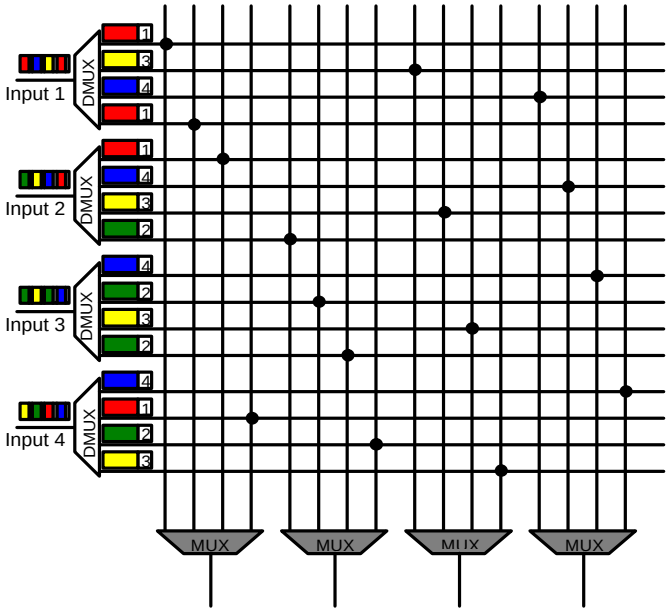

Figure 5: Principle of the channel multiplexing switch**.**

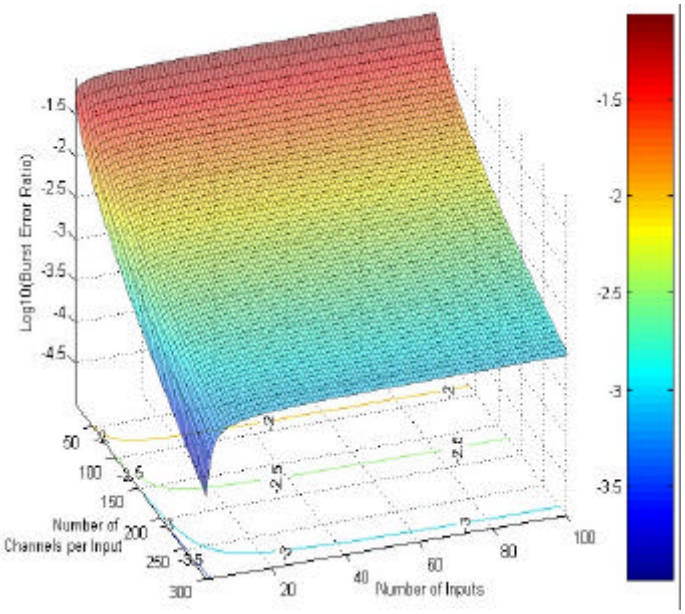

Figure 6: Burst Error Ratio with respect to the number of inputs and to the $N_{\text{input channels}}$.

Figure 6 highlights the theoretical influence of the number of switch input and output ports and the $N_{\text{input channels}}$ and $N_{\text{output channels}}$ per port on the burst error ratio generated in a system at 90 % load.

Whereas the losses generated by the channel multiplexing switch are insensitive to the number of switch's input and output ports (unless for a low number of inputs, which is out of scope of the scenario), the decrease of $N_{\text{input channels}}$ per switch's input increases these losses significantly.

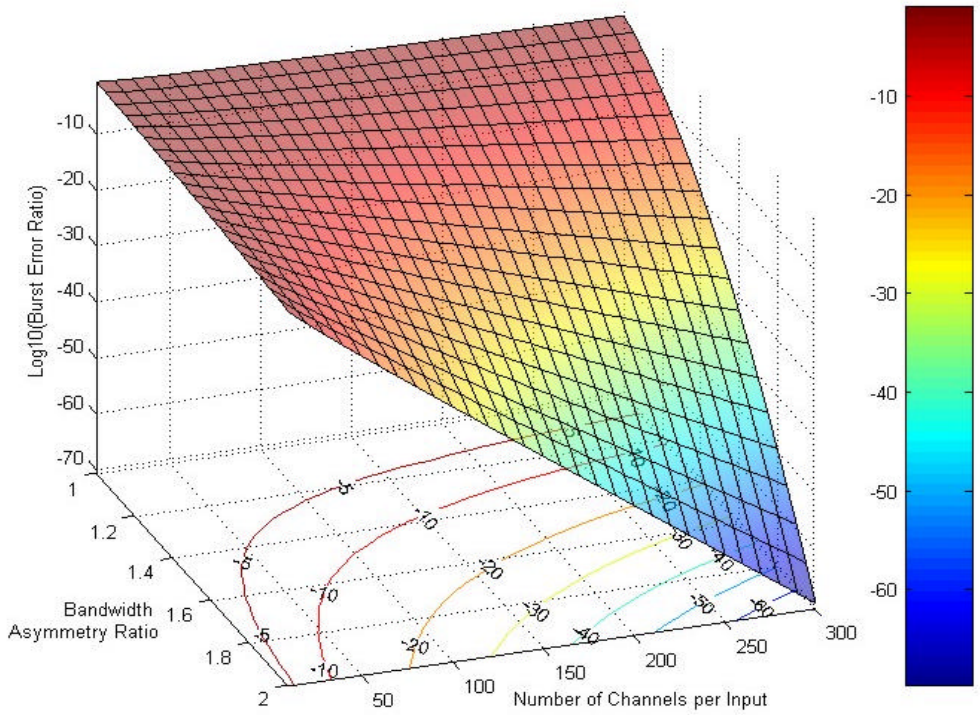

Figure 7: Burst Error Ratio generated by an on-board channel multiplexing switch loaded at 90% with 96 inputs and outputs as a function of the $N_{input\ channels}$ per input and the bandwidth asymmetry

As seen in Figure 6, even an high $N_{input\ channels}$ value is not sufficient to reach a very low loss probability. In this case, bandwidth asymmetry could be used to efficiently solve contention and decrease the losses generated by the switch (Figure 7). Bandwidth asymmetry amounts in assigning more channels per switch output than per switch input, and it is equivalent to low the downlink beam load. Nevertheless, this method should be carefully used, since the additional channels associated to the switch outputs are only used in case of contention situations. This means that the increase of the bandwidth asymmetry ratio decreases the losses due to contention in the switch output but decreases also the down-link bandwidth utilization ratio.

3.5 - ON BOARD BUFFER REQUIREMENT AND SCHEDULING:

In addition to the channel multiplexing technique, which displays relatively low losses when compared with classical crossbar switch architectures, a shared buffer should be used on-board to enable to reach a tolerable level of loss under the satellite traffic composition assumption. Figure 8 displays the loss ratio generated by the on-board switch with shared buffer with respect to the buffer's size for different traffic compositions (percentage of the overall traffic transmitted over C_1, C_2, C_4, and C_{16} channels). When no C_{16} channels are supported, a buffer containing roughly 10000 sampled and digitalized elementary bursts (carried over a single C_1 channel) should be foreseen to reach a good level of performance. Under the same hypothesis, the delay cumulative density function (CDF) due to the use of a shared buffer is represented in Figure 9, in data bursts duration. It is remarkable that the generated delays remain in any cases very low.

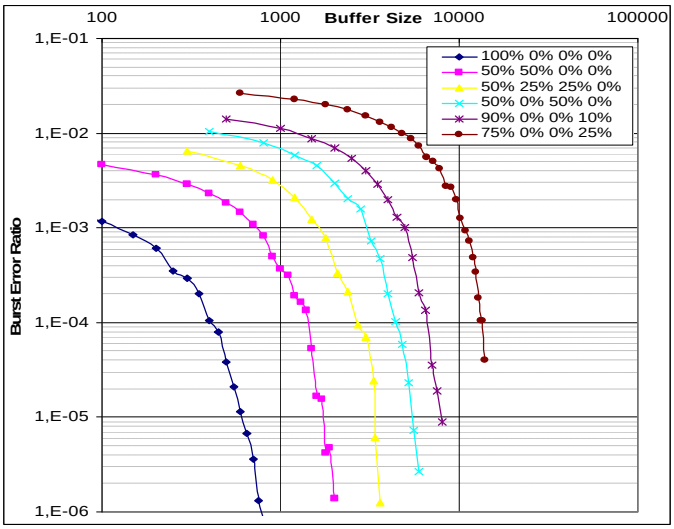

Figure 8: Burst Error Ratio as a function of the buffer size (shared buffer used) for a system with 96 beams, 2 sub-bands per beam, 78 C_1 channels per UL sub-band, 85 per DL sub-band, for different values of the burst bandwidth composition**.**

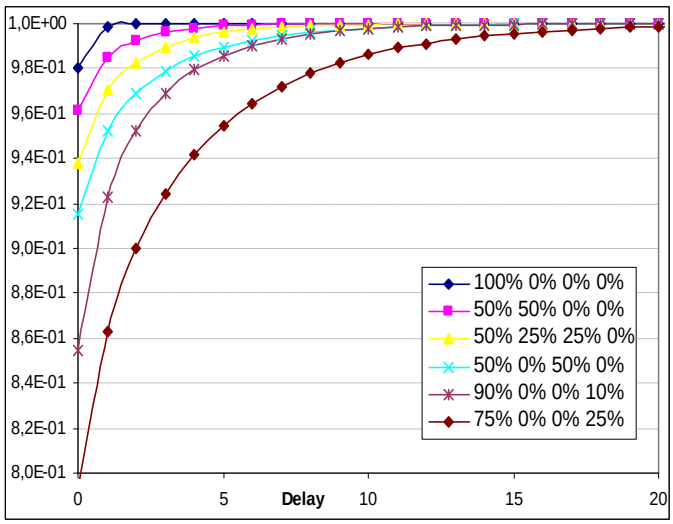

Figure 9: Cumulative Density Function of the bursts delay (shared buffer used) for a system with 96 beams, 2 sub-bands per beam, 78 C_1 channels per UL sub-band, 85 per DL sub-band, for different values of burst bandwidth composition.

In addition, traffic differentiation will be provided on-board. Thanks to weighted algorithm (e.g. Weighted Round Robin), it could be shown (not presented here) that it is possible to manage both packet loss free QoS (interactive and background) and delay free QoS (e.g. VoI).

3.6 - TERMINAL LIMITATIONS AND IMPACT AT SATELLITE SYSTEM LEVEL

Another source of losses in the considered satellite system could be due to the terminals processing capability. Indeed, receiving terminals should likely be able to simultaneously demodulate several carriers when bursts are simultaneously transmitted from different sending terminals.

Present day terminal suffers from the two following limitations:

- First, its frequency hopping capabilities are limited to tens of MHz (both in reception and transmission), so that a terminal can only demodulate carriers (and also emit over carriers) in a given sub-band of the whole frequency band associated with a beam.
- Second, a terminal is likely limited in the amount of carriers it can simultaneously demodulate (typically for tens of MHz).

As illustrated in Figure 10, the number of sub-band per beam (directly dependant on the terminal technology) have a deep impact on performance, and the smallest number of sub-band per beam is targeted .

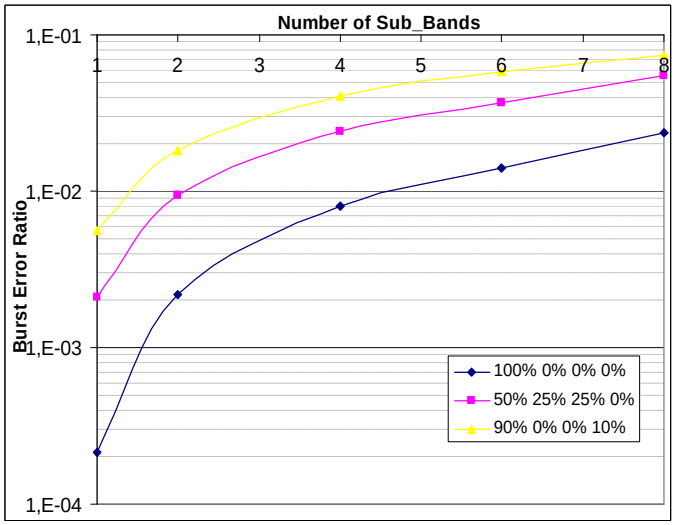

Figure 10: Burst Error Ratio as a function of the number of sub-bands for a system with 96 beams, 156 C_1 channels per UL beam, 170 per DL beam, no buffer.

In the considered satellite system, forecast in a near future have lead to select a terminal able to demodulate and decode all the carriers managed within a 125 MHz band, so in the scenario it is proposed to have 2 sub bands per beam.

4 - RBS PROCESSOR IMPLEMENTATION.

4.1 - RBS PROCESSOR DESCRIPTION.

Processor is supposed to manage base band signals. The neighbouring stages of the satellite payload being antenna feeds, amplifiers, down converters, beam forming are not presented in this paper (see also [7]). It is composed of two main parts: the first one is in charge of the useful data (wideband transparent processing-oriented) and the second one deals with the header and signalling flow (regenerative processing oriented).

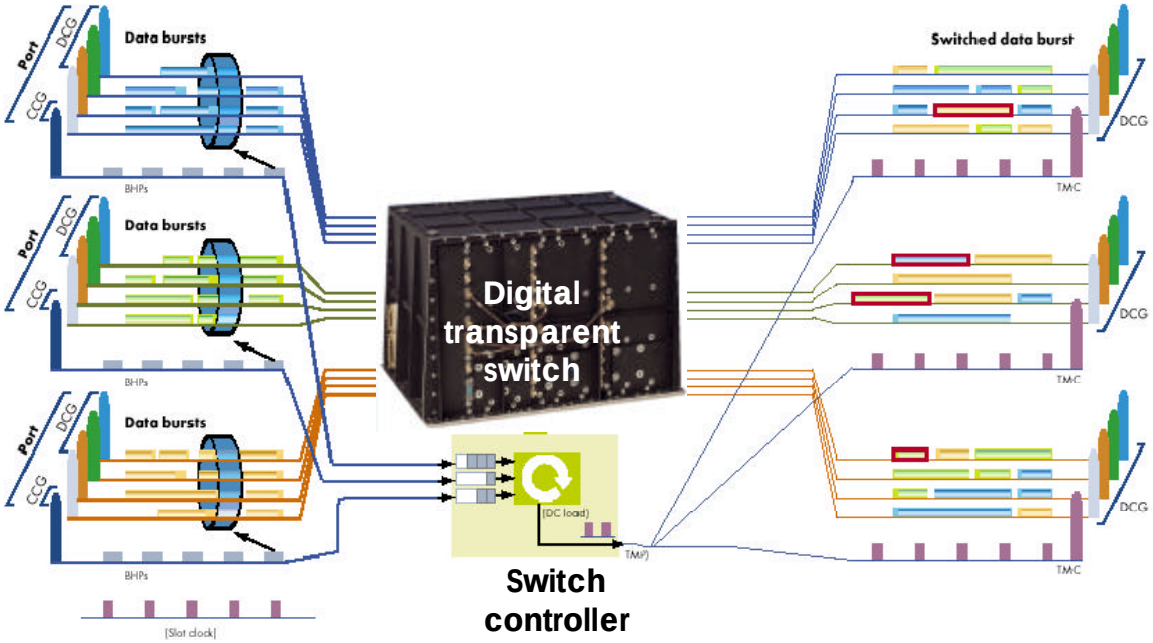

Figure 11: On-board RBS forwarding and controlling sections

For flexibility reasons, data and control channels frequency demultiplexing is done by digital filtering techniques, allowing channels reallocation at the packet speed, in line with meshed satellite networks requirements. Once demultiplexed by DEMUX, digital samples of data and control packet are respectively connected to transparent switch and 'demodulation & decoding' (DD) sections. Data channels sample are then multiplexed back by a MUX section. Once processed control packets (BHP, signalling), are regenerated with additional signalling if necessary and inserted into the MUX section.

4.2 - MULTI STAGE ULTRA FAST SWITCH.

Concerning the useful data conveying, the rate of samples to switch is roughly ~ 300 Gbits. Clearly, it is out of specification for existing single-stage switch-fabric chip set (that is around 80 Gbps, capacity being mainly limited by the maximum power dissipated by chip). Then, a multi-stage architecture could be proposed.

Under this architecture, samples from data channels are regrouped into micro-slot and serialized at the maximum possible rate into multi gigabit links (it corresponds to the first stage called time switching). Then, multi gigabits links are space switched (second and central stage) and time switched again in the last stage. For interconnect saving reasons (§ 4.5 -), it is proposed to regroup the first time switching stage with the DEMUX section

This architecture also supposes that high speed interconnects are feasible (for e.g. between different stage of the switch). Current works and demonstrations lead by A.Space and CNES on optical backplanes and interconnect [8], [9], confirm that this TST switch architecture is in line with future generation of interconnect solutions.

4.3 - THE ENABLING TECHNOLOGY: MULTI GIGA BIT TRANSCEIVERS.

The key technology used for managing high speed links is MGT (Multi gigabit transceiver), which promising improvements on power and integration are expected for the coming years.

At the emission or at the reception, MGT manages a specific link layer that is required for multi gigatbit transmission effects (dielectric loss, reflections, crosstalk, skew, T°). Generally, MGT includes Word insertion / detection, clock generation/recovery, error protection, equalization/pre-emphasis. In particular, multigigatbit ASIC to ASIC interconnects can be possible as well as board to board interconnects using the same MGT technology. Even in case of optical links (board to board or equipment to equipment interconnects) where MGT are used in addition with optical modules.

Figure 12 presents the influence of MGT power consumption on RBS processor mass and power, while keeping the same ASIC technology and system scenario, and points out the sensibility of processor characteristic with MGT. Integrated solution is clearly a key enabling solution.

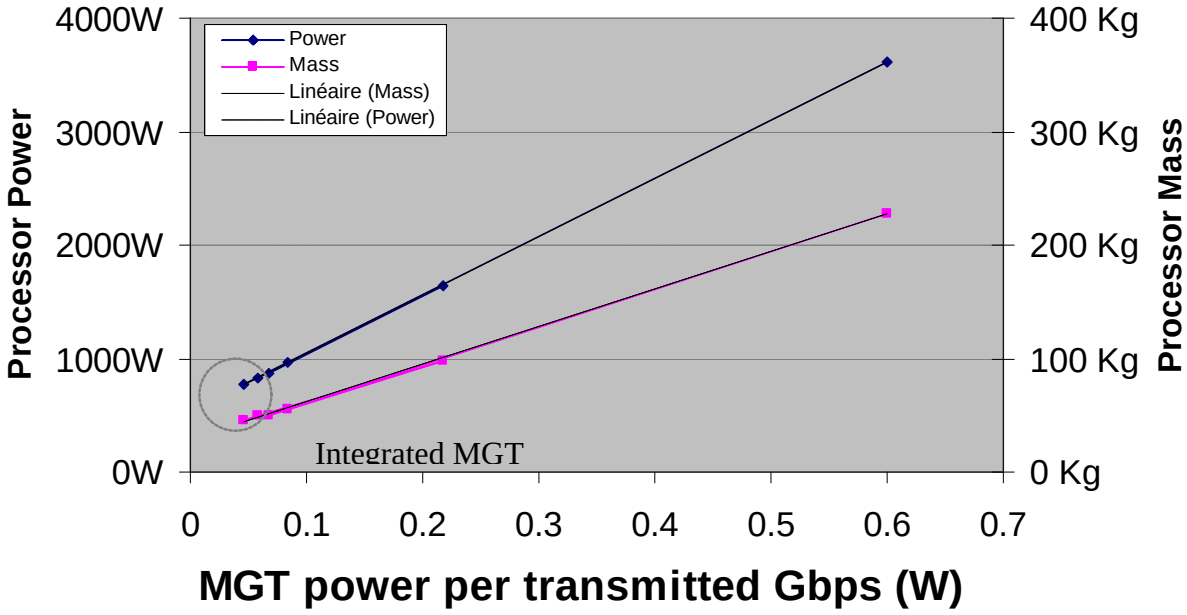

Figure 12 Power and mass dependence with MGT Generation.
(power per transmitted Gbps presented in **Erreur ! Source du renvoi introuvable.**)

4.4 - CHANNELS AND TIME AND SPACE SCHEDULING ALGORITHMS.

Once demodulated & decoded, headers are send to the processor controller section. This section is expected to be largely based on memory. Indeed, RAM containing routing tables, FIFOs and registers for sorting and queuing operations will be required.

Processor controller is also supposed to compute the time and space switching plan (=scheduling of the 3 stages Clos switch). This computation is not trivial, many literature exists, and algorithms can be classified into two groups “maximum” and “maximal” (or “heuristics”). Maximum algorithms always process the best arrangement but expected complexity and/or processing time are polynomial of the required connectivity. Even if performance is attractive, the high connectivity like ~16k could cause feasibility issue. The maximal group of scheduling algorithm (like iterative algorithms) is often used for terrestrial switching, and offers simplest implementation for high connectivity switches, but the counter part is the poor performance at high load ([10] , [11]).

4.5 - INTERCONNECTION AND BOARD MAPPING RECOMMENDATIONS.

As it is presented in Figure 14, the interconnection is important contribution of power budget, then board splitting is done in order to minimize interconnection cost. For example, it is preferable to host DEMUX and DD sections in the same board because DEMUX output rate (and then power) is around 16 times more than at DD output (see Figure 13). This consideration is also true for the board repartition of ADC or DAC, supposed to be the closest to the DEMUX ASIC chip. The conclusion is that having "specialized" board is power consuming because chip-to-chip or board to-board interconnect is costly. Conversely, an "on the flow" board design save interconnect power. This approach has been adopted to the RBS processor design presented in section 4.6 -.

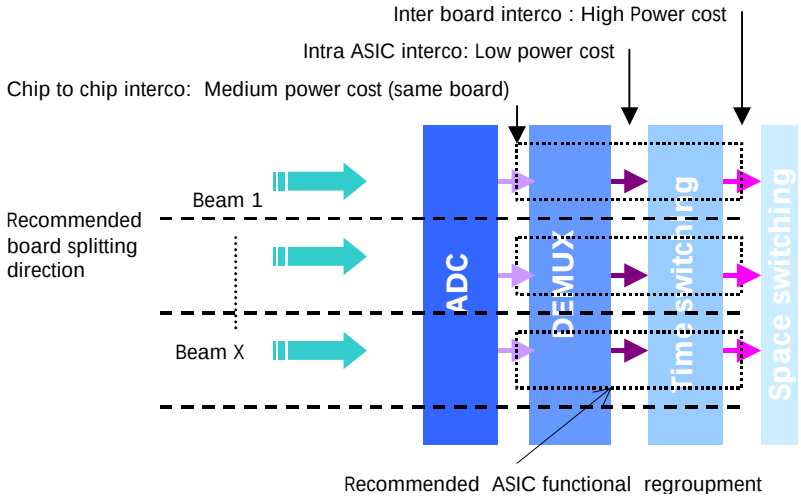

Figure 13 Recommendation on functional mapping into ASIC and board (2010 horizon techno)

4.6 - PROCESSOR ARCHITECTURE

Figure 14 presents an example of processor architecture at 2010 horizon mainly based on a future 0,9 um ASIC technology and associated typical MGT (derived from Xilinx Virtex 4). Circle chart presents the power repartition between, ADC/DAC (if any), ASIC and interconnect. It can be noticed that the switch controller board is ASIC (memory) intensive, while interconnect is the main power contributor (60%) on space switch board.

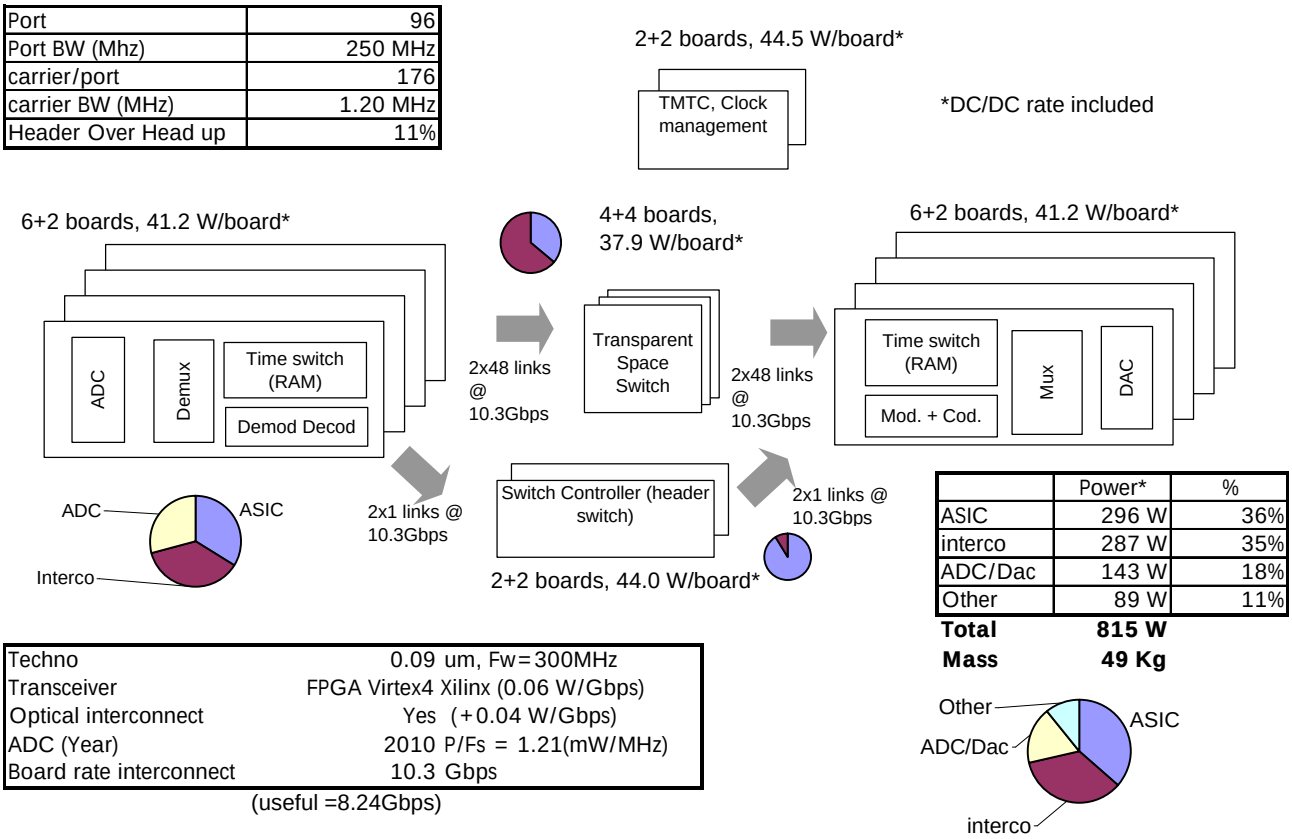

Figure 14 Processor main characteristics at 2010 horizon.

As it can be noticed, the cost from interconnection is about the same order than the power budget dedicated to ASIC. That is the reason why low power interconnect are absolutely necessary with the a Time-space-time switch architecture (see evolution with interconnect technology is presented Figure 12).

4.7 - CONTINUOUS TECHNOLOGICAL IMPROVEMENTS.

The ultra fast packet processor feasibility is also enabled by improvement of other contributing technologies: ASIC generation (core power consumption) and ADC/DAC. For the same system scenario, Figure 15 shows that power and mass improvement. It mainly come from ASIC technology evolution; with a gain of ~12 on processor power or mass in 12 years.

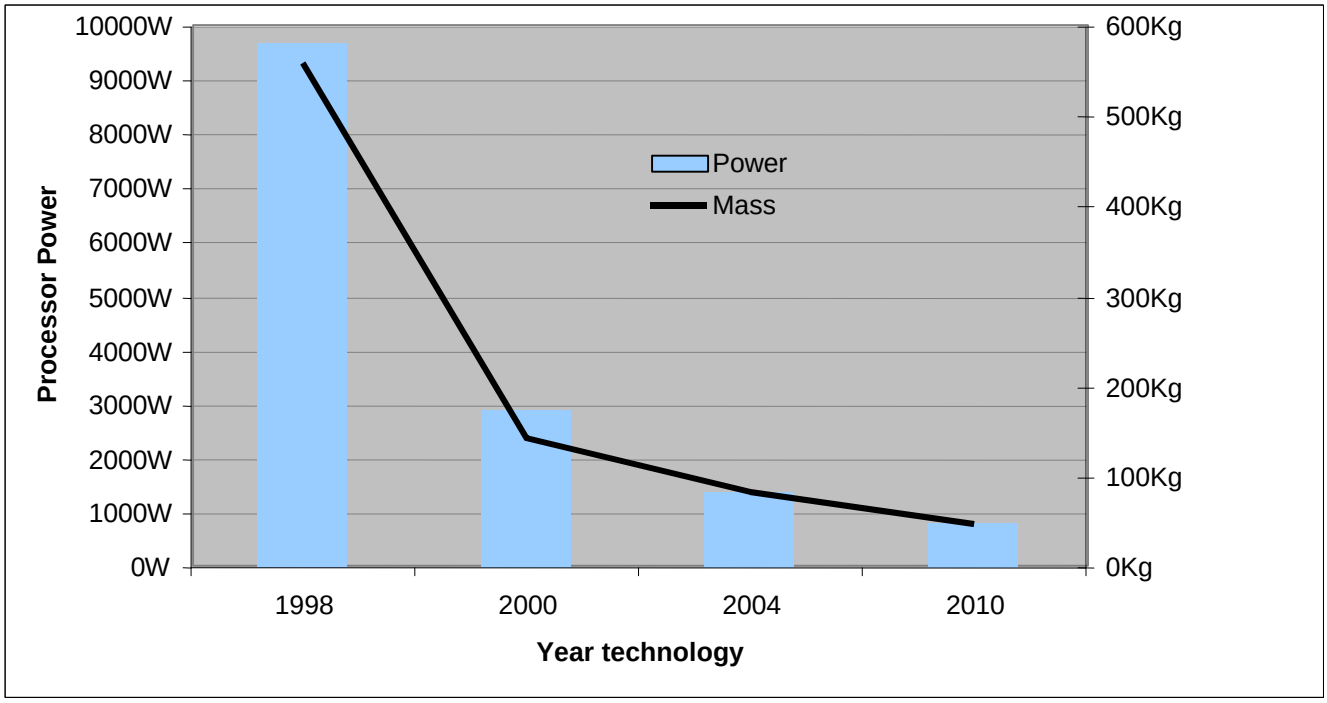

Figure 15 RBS power improvement with technology year.

Assuming a typical satellite platform with 12kW of DC Power, with the very approximate limitation of 10-20% of DC power to be delivered to the digital processor, feasibility of the proposed scenario should be possible starting from these years.

5 - CONCLUSION

Radio Burst Switching sums the interest of packet switching services with a relative the waveform independence of the data path. The potential gain on the embedded complexity thanks to a selective processing allows the satellite to propose wider band to switch than traditional regenerative solutions. This technique could be a promising solution compared to circuit switched systems for switching statistical traffic such as Internet traffic, connecting a high number of users. The broadband system scenario, dealing with hundreds GHz of switched bandwidth, was considered as unfeasible 5 years ago, it can be viewed now as realistic, thanks to integrated multigigabit transceivers MGT and ASIC technology improvements.

This concept is planned to be prototyped in 2006 in the frame of the ULISS project funded by ESA. In addition to hardware implementation of an ultra fast switch, this project also proposes the demonstration using an existing DVB-RCS test-bed. The aim is to demonstrate the ability of Radio Burst Switching to be integrated into a realistic satellite radio environment.

The ULISS project.

The ULISS (ULtra fast Internet Satellite Switching) project is 2 years long and is funded by the ESA ARTES program. The ULISS team is composed of four organizations in the European and Canadian space business: Alcatel Space (ASP), in France, is prime contractor and will bring its expertise in advanced telecommunication satellite within its research department. Alcatel R&I, in Germany, will bring its broad expertise in developing innovative solutions for the routers of terrestrial terabit networks. Deutsches Zentrum für Luft-und Raumfahrt (DLR), in Germany, will bring its high experience in advanced communication satellite systems and communication technologies. Lyrtech, in Canada, will bring its experience in digital signal processing engineering and design of processing unit based on DSP and FPGA.

6 - BIOGRAPHIES

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7 - ACRONYMS

ADC	Analogue to Digital Conversion
ASIC	Application-Specific Integrated Circuit
BHP	Burst Header Packet
CC	Control Channel
CCG	Control Channel Group
CSC	Common Signalling Channel
DAC	Digital to Analogue Conversion
DC	Direct Current, Data Channel
DCG	Data channel Group
GT	Guard Time
IP	Internet Protocol
MGT	Multi gigabit Transceiver
NCC	Network Control Center
OBS	Optical Burst Switching

PID	Packet Identifier
QoS	Quality of Sercive
RBS	Radio Burst Switching
SAC	Satellite Access Control
SS-TDMA	Satellite Switched Time Division Multiple Access
SYNC	Synchronization
TDM	Time Division Multiplex
TST	Time Space Time
ULISS	Ultra fast Internet Satellite Switching
VCI	Virtual Channel Identifier
VPI	Virtual Path Identifier
WDM	Wavelength Division Multiplexing

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